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Tunable Fiber Bragg Grating Based Optical Packet Switch

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Abstract—In the approaching years, optical packet switching (OPS) will be a promising data transfer method. Contention between packets is a major issue in OPS, and it occurs when multiple packets try to use the same output link. Optical packet switches are utilized for contention resolution,where except one other contending packets are stored. In this paper, a switch design is proposed where tunable fiber Bragg gratings (TFBGs) are used in the realization of switch.The buffer is recirculating in nature in this design, with no control inside the buffer. The switch's performance is assessed at both the physical and network layers. In comparison to the previous re-circulating switch design, the new design was determined to be substantially better.

Keywords—TFBG, EDFA, Circulator, OPS

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I. Introduction

The demand for higher bandwidth is increasing continuously. This continuous demand gives rise to the exploration of optical packet switching. In the last few years lot of research have been done for the implementation of the optical packet switching. In the dense telecom infrastructure, the connection among two nodes generally employ a low-degree of fan-in, but have a high capacity of bandwidth that is in the range of gigabytes to terabytes every second. To manage such high capacity links, in optical fiber, Dence Wavelength Division Multiplexing techniques are employed that multiplexes several wavelength streams into a single fiber sheath. Due to this, parallel wavelengths can be employed simultaneously on the fiber links. Once the client application sends data to the edge nodes, the high capacity links forms an end-to-end path to the receiver edge through the core backbone network. There exist several benefits of optical packet switching over electronic packet switching, but there are two hurdles in the implementation of OPS one is the lack of optical RAMs and the other is the unavailability of TWC. In optical packet switching, FDLs are used for the temporary packet storage and these FDLs have a great packet storing capacity. In an optical packet switching system, an effective buffer is essential for the proper packet synchronization and for avoiding collision among all paths. In OPS system the best option for buffer technique is the application of optical fiber delay lines in the core of the switch as depicted in [1-7]. Each packet in an optical switched network experiences a combined movement in both electrical and optical domain, and thus the incurred delays and power usage varies through the core and the edge networks. To manage and compensate the variable delays at separate network points, buffers are strategically placed in both the core and edge networks. Ideally, the size of the buffer needs to be sufficiently large to minimize the packet losses, but practically large buffer sizes are not available. Moreover, the contention resolution schemes needs to be addressed intelligently in electrical switches by storing the packets in the buffers with no effect of switching patterns.

In this paper, an optical packet switch design is discussed which can be effectively utilized in the core network. The buffer is created using FDLs, and tunable Fiber Bragg grating.

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II. Switch Design

The presented design falls under the category of broadcast and select type switch. In the switch two EDFAs are placed; one after combiner to compensate the loss of the straight through packets. Second EDFA is placed inside the loop to compensate the loss of re-circulating packets.For the straight through packets tunablefiber Bragg gratings remain transparent, and at the output of the switch particular tunable filter (TF) tunes its wavelength to accept the packet while other TF discard it. Input TWC make sure that the wavelengths of the packets passing through the switch falls under the tuning range of TFBGs and TFs. Contending packets are first passed though the circulator (a device which allow data propagation in anti-clockwise direction) and they will be reflected by any of the TFBGs and enter loop and passed though the EDFA and again appear at circulator, if contention has resolved for particular packet, then the corresponding TFBGs changes its wavelength and becomes transparent for the packet and it appear at the output of the switch where it is accepted by appropriate TF. But if contention persist, then TFBGs will not change its wavelength and again packets will be reflected back to loop, this process continues till contention resolves.

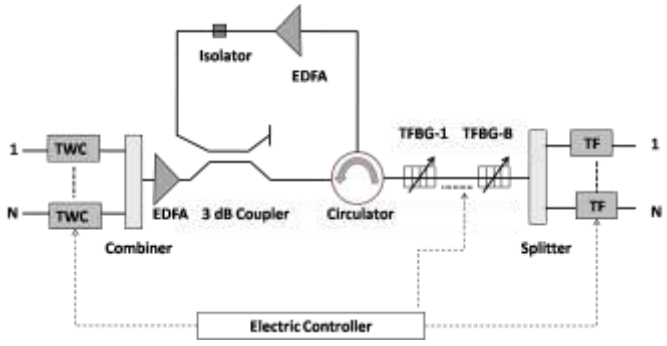

Fig. 1: Schematic of the proposed optical switch

The number of TFBGs will decide the buffering capacity. The length of fiber loop is equal to packet duration.In the switch design two EDFAs one at the input of the switch while in the second EDFA is placed inside the fiber loop. It is assumed that input EDFA compensate the power loss of the straight through packets, while EDFA in the loop compensate the power loss inside the buffer. The placement of the EDFA is done optimally, as this design will maintain the signal power, while noise gets reduced as it passes through various switch components.

In this design, in the buffer no controlling is required and controlling of the straight through and buffered packets is done using TunableFiber Bragg Gratings. The numbers of buffer gratings are equal to the number of TFBBGs.

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III. Buffer length and power budget analysis

Buffer Length

The fiber length in the buffer is equal to the equivalent packet length. The length of the fiber is calculated using the expressions

$$L = \frac{cb}{nB_R}$$

Where c is the speed of light, n is the refractive index, b is the packet length in terms of bits and B_R is the bit rate.At the data rate of 40 Gbps, for 1000 bits packet is 5.17 meter. At the similar data rates, for 5000 and 10000 bits packets length is 25.86 meter and 51.72 meter respectively.

Power analysis

In this architecture, power received at the output of the switch when both input and buffer amplifiers are used is

$$P_{out} = bP_{in}A_{in}G_{in} + n_{sp}(G_b - 1)h\nu B_o \sum_{i=1}^{K}\left(A_bG_b\right)^i A_T / A_{in} + n_{sp}(G_{in} - 1)h\nu B_o A_T / A_{in} \quad (1)$$

Where, the input (A_{in}), buffer (A_b), and total loss (A_T) is given by

$$A_{in} = L_{TWC}L_{Com}$$

$$A_b = L_{Cir}L_{3dB}L_{Cir}L_{Iso}L_{TFBG1}L_{EDFA}$$

$$A_T = L_{TWC}L_{Com}L_{3dB}L_{Cir}\left(L_{TFBG}\right)^B L_{Split}L_{TF}$$

The gain of the amplifier at the input of the switch is G_{in} and gain of the EDFA in the buffer is G_b respectively.The value used for the considered parameters are detailed in Table 1. We consider that $A_{in}G_{in}$=1

If loss of the buffer is fully compensated by the gain of EDFA, i.e.,A_bG_b=1 then the equation 1, can be re-written as

$$P_{out} = bP_{in} + Kn_{sp}(G_b - 1)h\nu B_o A_T / A_{in}L_{EDFA} + n_{sp}(G_{in} - 1)h\nu B_o A_T / A_{in} \quad (2)$$

Noise analysis

Due to the beating phenomenon and thermal effect the below mentioned noise components are generated at the receiver [14]:

Shot noise

$$\sigma_s^2 = 2qRPB_e$$

ASE-ASE beat noise

$$\sigma_{sp-sp}^2 = 2R^2P_{sp}(2B_o - B_e)\frac{B_e}{B_0^2}$$

Sig-ASE beat noise

$$\sigma_{sig-sp}^2 = 4R^2P\frac{P_{sp}B_e}{B_0}$$

Shot-ASE beat noise

$$\sigma_{s-sp}^2 = 2qRP_{sp}B_e$$

Thermal noise

$$\sigma_{th}^2 = \frac{4K_B T B_e}{R_L} \qquad (3)$$

In the above expressions P an P_{sp}isrepresnetd by

$$P = bP_{in}$$

and

$$P_{sp} = Kn_{sp}(G_b - 1)h\nu B_o A_T / A_{in} L_{EDFA} + n_{sp}(G_{in} - 1)h\nu B_o A_T / A_{in} \qquad (4)$$

The total noise variance for bit b is

$$\sigma^2(b) = \sigma_s^2 + \sigma_{sp-sp}^2 + \sigma_{sp-sig}^2 + \sigma_{s-sp}^2 + \sigma_{th}^2 \qquad (5)$$

The bit error rate is evaluated using

$$BER = Q\left(\frac{R\left(P_1 - P_0\right)}{\sigma_1 + \sigma_0}\right)$$

Where, Q(.) is error function, and R is responsivity of the receiver.

TABLE 1: LIST OF PARAMETERS

Parameters	Value
Size of the switch	4
Population inversion factor	1.1
Gain of the amplifier	20dB
Speed of light	3x108
Refractive index of fiber	1.45
Loss of Isolator	0.5 dB
Responsivity	1.28 A/W
Electronic charge	$1.6\times10^{-19}C$
Electrical bandwidth	10GHz
Optical bandwidth	20GHz
TWC insertion loss	2.0 dB
Loss of 3dB coupler	3.0 dB
Loss of the Circulator	1.0 dB
Loss of Tunable Filter	1.0 dB
Loss of TFBG	1.0dB
Loss EDFA	1.0 dB
Wavelengths	ITU Grid
Temperature	300K
Boltzmann Constant	1.38x10-23
Plank Constant	6.6x10-34
Load Resistance	300 ohm
Loss (Combiner/Splitter)	6.0 dB
FBG Insertion Loss	0.5 dB
Fiber Loss	0.2 dB/km
FBG reflectivity	0.995

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Using the above formulation, in the buffer number of circulations are calculated such that when packet received at the output has BER$\leq 10^{-9}$. In the calculation buffer is varied as 4 and 8.
In table 2, number of circulations at different power levels is shown while buffering of 4 packets. It is clear from the table that as the power increases; packets can stay in the buffer for more number of circulations. At the power of 7 micro-watts, 5 circulations is allowed which increases to 27 circulations at the power of 20 micro-watts. In general buffer with capacity of four packets only four circulations will require to utilize full buffer capacity. Thus a power level of 7 micro-watts would be sufficed. But in pritorized traffic where low priority packet may stay longer in the buffer, then a large number of re-circulation may be desirable.
In the similar context, BER vs power level is detailed in Table 3, for N=4 and B=4. Here, as the power increases the BER also improves. As in most of the optical communication system the acceptable BER limit is BER$\leq 10^{-9}$. Thus again the minimum required power level is of 7 micro-watts. However for the BER$\leq 10^{-12}$, the minimum required power level is 9 micro-watts.

Table 2: Power vs. circulations for N=4 and B=4

N=4 and B=4	
Power (micro-watts)	**Circulations**
5	1
6	3
7	5
8	6
9	8
10	10
11	11
12	13
13	15
14	16
15	18
16	20
17	22
18	23
19	25
20	27

Table 3: Power vs. BER for *N*=4 and *B*=4

***N*=4 and *B*=4**	
Power (micro-watts)	**BER**
5	2.41×10^{-7}
6	1.48×10^{-8}
7	9.18×10^{-10}
8	5.72×10^{-11}
9	3.58×10^{-12}
10	2.24×10^{-13}
11	1.41×10^{-14}
12	8.88×10^{-16}
13	5.60×10^{-17}
14	5.33×10^{-18}
15	2.23×10^{-19}
16	1.41×10^{-20}
17	8.91×10^{-22}
18	5.63×10^{-23}
19	3.56×10^{-24}
20	2.25×10^{-25}

In table 4, number of circulations at different power levels is shown while buffering of 8 packets. At the power of 6 micro-watts, 6 circulations are allowed which increases to 66 circulations at the power of 20 micro-watts. Thus by increasing the buffer size from 4 to 8, the power is reduced by 1 micro-watts, this happens due to the large loss suffered by the noise. However, the signal power remains same. Thus SNR improves slightly, thus in turn improves the BER.

Table 4: Power vs. circulations for *N*=4 and *B*=8

***N*=4 and *B*=8**	
Power (micro-watts)	**Circulations**
5	2
6	6
7	10
8	15
9	19
10	23
11	27
12	32
13	36
14	40
15	45
16	49
17	53
18	57
19	62
20	66

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In the similar context, BER vs power level is detailed in Table 5, for N=4 and B=8. For the acceptable BER limit is BER≤10^{-9}, the required power is of 6 micro-watts. Thus the minimum power level is reduced by 1 micro-watts. However for the BER≤10^{-12}, the minimum required power level is 9 micro-watts.

Table 5: Power vs. BER for *N*=4 and *B*=8

***N*=4 and *B*=8**	
Power (micro-watts)	**BER**
5	1.03×10^{-7}
6	5.36×10^{-9}
7	2.80×10^{-10}
8	1.47×10^{-11}
9	7.73×10^{-13}
10	4.08×10^{-14}
11	2.16×10^{-15}
12	1.14×10^{-16}
13	6.05×10^{-18}
14	3.21×10^{-19}
15	1.70×10^{-20}
16	9.05×10^{-22}
17	4.80×10^{-23}
18	2.55×10^{-24}
19	1.36×10^{-25}
20	7.20×10^{-27}

COMPARSION WITH RE-CIRCULATING TYPE BUFFER DESIGN

In Table 6, various re-circulating type buffer switch designs are compared. In [6] buffer is created using large numer of compenents, therefore total loss of the switch is very large, thus for correct operation of the switch required amount of power is 3 mW. The buffer design is simplified in [13] thus power level reduces to 0.1 mW. In recent design [14], loss of the switch is minimized using arrayed waveguide grating and the required amount of power is 16 µW. In this paper buffer is fruther simplified without any components thus required amount of power further reduces to 10 µW.

Table 6: Comparison of switch design

Reference/Year	**Power level**
[6], 2009	3 mW
[13], 2008	0.1mW
[14], 2019	16 µW
Proposed	10 µW

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simulation results

In the previous section, switch performance is evalueted at the physical layer in terms of bit error rate. However, in networks data is transported in the forms of packet and we aim to high packet throghput. In this section, packet loss perfromance is measured. In the switch modelling Monte Carlo simulaton is performed and consider that arrival of packet is random, and at any input packet can arrive with probability '*p*' and arriving packet choose any of the output with equal probability '1/*N*'. Further, it is also cosnidered that the arrival packets are independent to each other.

For the switch configurations of N=4, B=4, 8, 16 the simulated results for packet loss probability is shown in Figure 2. It can be seen from the figure as the buffer size increases the packet loss probability decreases. The packet loss probability at the load of 0.7 for B=4 is 10^{-2} for B=8 the packet loss probability is 5×10^{-4} and that for B=16 the packet loss probability is 3×10^{-7}. Thus by increasing the buffer size from 4 to 16 the packet loss probability is improved by the factor of 10000.

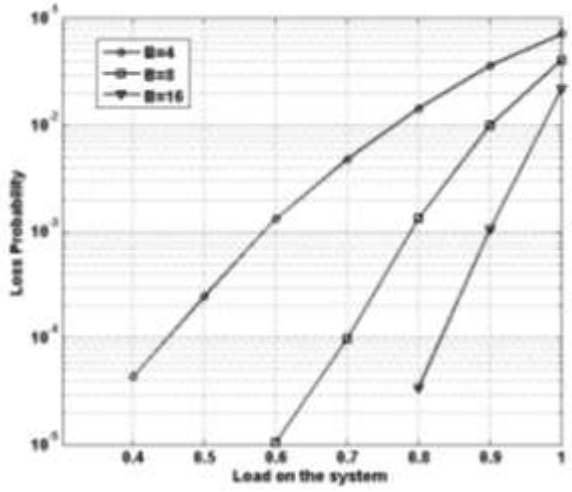

Fig. 2: Packet loss probability vs. load for N=4, and with variable buffer

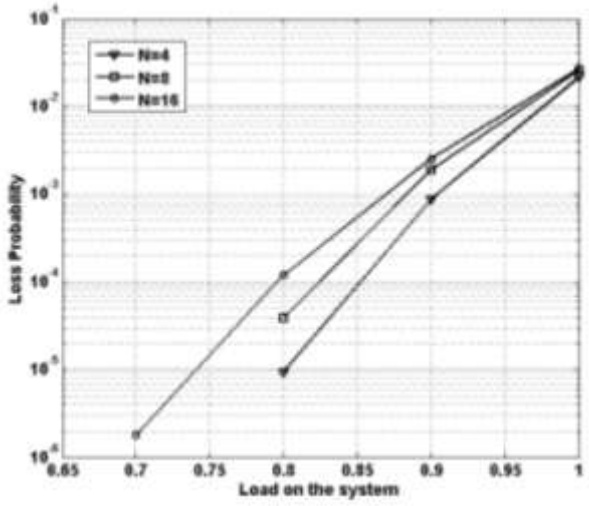

Fig. 3: Packet loss probability vs. load for variable inputs and fixed buffer

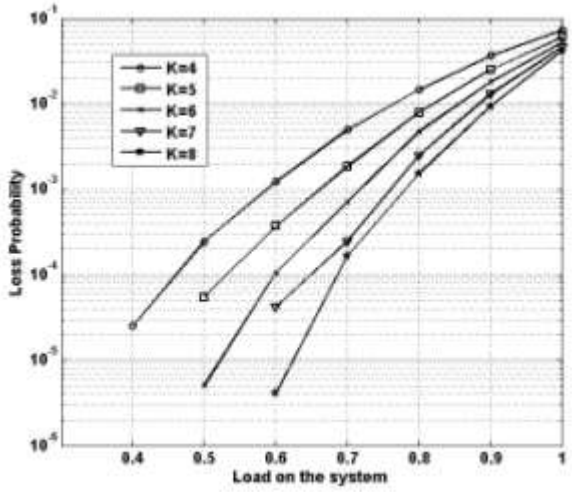

Fig. 4: Packet loss probability vs. load for N=4, under different re-circulating counts

Figure 3 shows the packet loss rate vs. load for different numbers of inputs while keeping the buffer at a fixed level of 16 packets. As can be seen in the graph, as the switch size grows, the chance of packet loss reduces. The packet loss probability at the load of 0.8 for N=4 is 10^{-5} for N=8 the packet loss probability is 5×10^{-5} and that for N=16 the packet loss probability is 1.1×10^{-4}.
Figure 4 shows packet loss rate vs load with different numbers of re-circulations while keeping the buffer at the same level of 8 packets. The re-circulation restrictions, as shown in the diagram, have a significant impact on the switch's overall performance. As a result, the input packet's power should be kept high enough to allow full buffer utilisation notwithstanding any re-circulation limits.

IV. Conclusions

This work presents comprehensive design and analysis of a TFBG based optical node switch which can efficiently work with OPS. The design on an efficient optical switching system is a tough problem, as various design components are interrelated. The major findings of the work are as under:

- Design modifications in OPS node architecture are presented such that switch can work more efficiently even at low power levels.
- The power budget assessments of the switch in terms of loss, power, and noises are presented, and the minimal signal power that may be correctly received at the output is estimated.
- In optical packet switching physical layer analysis (BER) is very important in designing of an efficient switching system. Hence switch BER is obtained under various switch size and buffering conditions. It has been found that for N=4 and B=4, the minimum amount of power is 7μW.
- Switch performance is measured at the network level in terms of packet loss probability. The results show that very low packet loss of 10^{-6} is attainable.
- The switch design is also affected by the bit rate and the quantity of bits in a packet.

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